

Claims 1-4, 6-13, 15-25, 27-35 and 37-40 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Derrick (U.S. Patent No. 5,872,980) in view of Perotto (U.S. Patent No. 5,630,130), and claims 5, 14, 26 and 36 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Perotto in view of AAPA. The following clear errors in the Examiner's rejection are noted.

Regarding claim 1, the Examiner provides different grounds of rejection in the Final Action and the Advisory Action, both of which are in error. In the Final Action, the Examiner asserts that Derrick teaches "a sequence of mutexes associated with a resource", citing col. 7, lines 1-2 of Derrick in support. The Examiner's assertion is clearly incorrect. The cited lines recite "a plurality of semaphores", but each of these semaphores is for a separate resource. According to Derrick, each shared resource has exactly one associated semaphore, and each semaphore corresponds to exactly one shared resource. The one-to-one relationship between semaphores and resources is repeatedly taught throughout Derrick (see, e.g., col. 6, line 65 – col. 7 line 10, col. 3, lines 55 – 63, col. 5, lines 36 – 39, col. 7, lines 24 – 28 of Derrick, reproduced in Applicant's response to the Final Action). The Examiner does not refute Applicant's arguments regarding this limitation in the Advisory Action. Instead, in the Advisory Action, with respect to the same limitation, the Examiner asserts that Perotto teaches the limitation, citing col. 1, lines 64-65, col. 5, lines 5-8 and col. 5, lines 10-12 of Perotto in support. The Examiner is again incorrect. The cited lines of Perotto are:

The concurrent execution of tasks by a microprocessor is conventionally done by means of a software mechanism called a scheduler. Such a mechanism is realized as a series of instructions stored in a ROM, and manages the above sequencing of the diverse tasks performed by the microprocessor. (Perotto, Col. 1, lines 60-65)

The ALU 11 and the RAM 12 are shared resources and can be accessed by all tasks executed by the controller 1. Semaphores are used to control access to the shared resources of the controller 1 in the following manner. When a task uses a shared resource, a bit in a selected data register is set busy. When this task has finished using the shared resource, this bit is set free. The state of this bit is tested by all tasks wishing to access a shared resource, and if the bit has been set busy by earlier task, the later task must wait until the bit is set free. (Perotto, Col. 5, lines 3 – 12)

Perotto does teach "semaphores used to control access to the shared resources of the controller". However, there is no teaching or suggestion, in the cited lines or anywhere else in Perotto, of a "sequence of mutexes associated with a resource". The "sequencing of diverse tasks" cited by the Examiner in the Advisory Action refers to operations of a "scheduler", and has nothing to do with any given resource having a sequences of mutexes associated with it.

Further with respect to claim 1, in the Final Action the Examiner asserts that Derrick teaches “to make a determination whether the sequence includes a previous mutex”, and cites col. 7, lines 36 – 40 of Derrick in support. (In the Advisory Action, the Examiner addresses this particular limitation in combination with other limitations, as discussed below.) The cited lines of Derrick are:

a lock and identification field, said lock and identification field adapted to identify which, if any, of the plurality of devices owns the shared resource corresponding to the semaphore which corresponds to the memory location (Derrick, col. 7, lines 36 – 40)

Clearly, there is no suggestion of a sequence of mutexes in the cited lines, much less of “making a determination of whether the sequence includes a previous mutex”, as recited in claim 1.

Still further with respect to claim 1, in the Final Action, the Examiner asserts that Derrick teaches “if a result of the determination is positive, to attempt to lock the previous mutex in the sequence, wherein the requesting thread is suspended if the previous mutex is already locked until the previous mutex is unlocked in response to a previous thread finishing access to the resource” at col. 8, lines 24 – 29. The Examiner is mistaken in this interpretation of Derrick as well. The cited lines are:

blocking access by a requesting device to the semaphore corresponding to the one address field which corresponds to the one memory location if the lock and identification data indicate that the requesting device does not own the shared resource and another of the plurality of devices owns the shared resource. (Derrick, col. 8, lines 24 – 29)

The cited lines of Derrick clearly do not teach responding to a determination that a sequence of mutexes (of which one mutex has been locked and allocated to a requesting thread) includes a previous mutex by attempting to lock the previous mutex in the sequence. In the Advisory Action, the Examiner suggests that Perotto (rather than Derrick) teaches this limitation, citing col. 5, lines 9-10 (reproduced above) in support. However, the cited lines also clearly do not teach the limitation in question.

For at least the reasons above, the rejection of claim 1 is not supported by the prior art and removal thereof is respectfully requested. Independent claims 10, 19, 22 and 32 each recite limitations using language similar to that of claim 1, and are also believed to be in condition for allowance for similar reasons.

In the Advisory Action, the Examiner also addresses Applicant’s arguments with respect to dependent claim 4, suggesting that Perotto teaches the limitation “wherein the mechanism includes an internal mutex operable to protect the locking of the mutex allocated to the requesting thread” because

“Perotto teaches semaphores (col. 5, line 5)”. However, Perotto does not teach one mutex being used to protect the locking of another mutex. Accordingly, the rejection of claim 4 is also clearly incorrect.

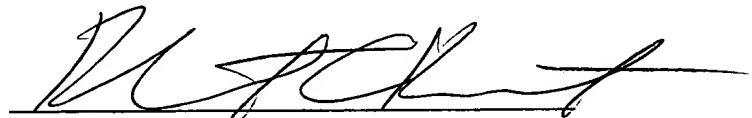
Furthermore, neither in the Final Action nor in the Advisory Action has the Examiner ever even attempted to respond to Applicant’s arguments regarding claims 6-9, 15-18, 27-30 and 37-40 as asserted in Applicant’s previous responses. Please see Applicant’s response to the Final Action for additional arguments with respect to a number of the dependent claims.

In light of the foregoing remarks, Applicant submits the application is in condition for allowance, and notice to that effect is respectfully requested. If any extension of time (under 37 C.F.R. § 1.136) is necessary to prevent the above referenced application from becoming abandoned, Applicant hereby petitions for such an extension. If any fees are due, the Commissioner is authorized to charge said fees to Meyertons, Hood, Kivlin, Kowert & Goetzel PC Deposit Account No. 501505/5681-67700/RCK.

Also enclosed herewith are the following items:

- ☒ Return Receipt Postcard
- ☒ Notice of Appeal

Respectfully submitted,



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